Distributed FPGA-based smart camera architecture for computer vision applications

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Abstract: **Smart camera networks (SCN) raise challenging issues in many fields of research, including vision processing, communication protocols, distributed algorithms or power management. Furthermore, application logic in SCN is not centralized but spread among network nodes meaning that each node must have to process images to extract significant features, and aggregate data to understand the surrounding environment.**

In this context, smart camera have first embedded general purpose processor (GPP) for image processing. Since image resolution increases, GPPs have reached their limit to maintain real-time processing constraint. More recently, FPGA-based platforms have been studied for their massive parallelism capabilities. This paper present our new FPGA-based smart camera platform supporting cooperation between nodes and run-time updatable image processing. The architecture is based on a full reconfigurable pipeline driven by a softcore.

I. Introduction

Smart Camera Networks (SCNs) is an emerging research field which represents the natural evolution of centralized computer vision applications towards full distributed systems. Indeed, in SCNs the application logic is not centralized, but spread among network nodes: every SCN node has the capability to pre-process images in order to extract significant features. In a such scenario, a strong cooperation between nodes is necessary, as well as the possibility of having pervasive and redundant SCN devices [1].

In this context, many hardware architectures for visual sensors network have been proposed [2]. Most existing platforms are based on GPP units [3] because this kind of architectures offers high level programming and modern embedded processors provide good performances. Despite this, embedded processors cannot meet real-time processing constraints when image sensor resolution increases.

On the other side, FPGA-based architectures which offering more massive computing capability than GPPs have been studied for implementing image processing applications on smart camera nodes [4]. However, if the introduction of FPGAs can address some performance issues in smart camera networks, it introduces new challenges concerning programmability of nodes, hardware abstraction and network management.

This work presents a FPGA-based platform offering high-capacity for image processing, but also being fully configurable and updateable. The proposed architecture is inspired by the Internet of Things, where all device nodes (including low-end ones) are addressable, and their *resources* may represent sensors, actuators, combinations of values or other information, eligible to be manipulated in M2M and H2M. FPGAs are therefore considered as publishers of Internet resources, addressable as URIs by means of application layer protocols like HTTP and COAP [5].

II. Hardware Architecture

The smart camera architecture used in this paper is a FPGA-based platform developed at our institute and called DreamCam [6] (Fig. 1). This smart camera consists of 5 stacked boards. This modular architecture allows us to easily adapt to new functions. For instance, different communication board have been designed and the switch from USB to Giga-Ethernet is trivial.

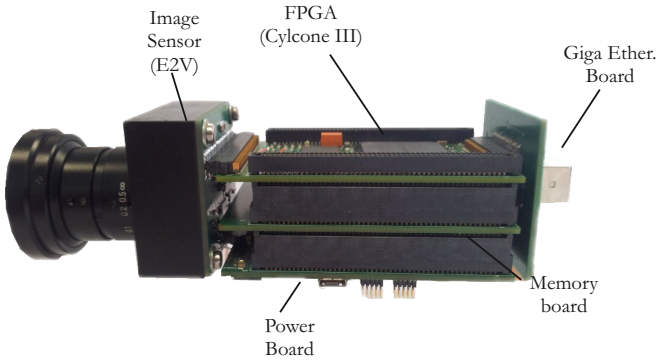

Fig. 1: DreamCam system

DreamCam platform is equipped by a 1.3 Mpixels CMOS image sensor from E2V, supporting sub-sampling/binning and multi regions of interest (ROIs). The processing core is a FPGA Cyclone-III EP3C120 FPGA manufactured by Altera. This FPGA is connected to 6x1MBytes of SRAM memory blocks wherein each 1MB memory block has a private data and address buses (hence programmer may address six memories independently). Fig 2 proposes the internal FPGA architecture. Two IPs (Intellectual property) have been designed to control the image sensor and the communication device. Thus, the pixel flow is processed by the configurable processor and results are ressources accessible via the internet network. The system management is performed by a softcore (NIOS II). At run-time, the softcore can specify Ethernet configuration (MAC and IP address), image sensor configuration (resolution, frame rate, ROI) and configures the processing block.

This block is composed by a pipeline of simple processing elements called *Elab* which can be interconnected via mod-

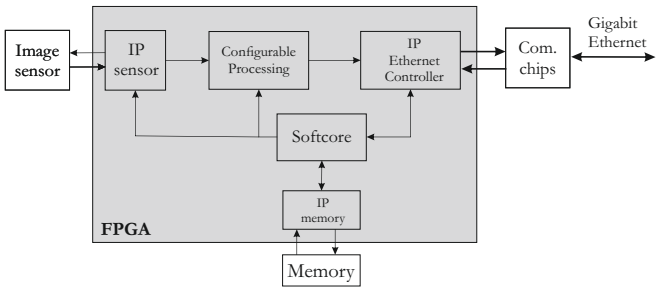

Fig. 2: FPGA logical architecture

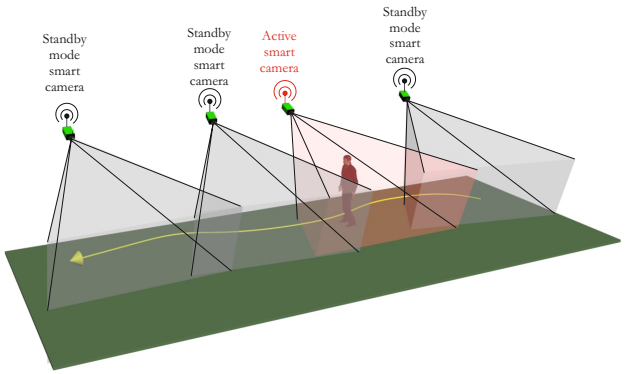

Fig. 4: Distributed target application

ules called *RouteMatrix* (Fig. 3). The processing element can be thresholding, convolution, histogram computation,... and the interconnection (*RouteMatrix*) can be viewed as multiplexer controlled by the softcore. In this way, each node (smart camera) can be configure via the network and provides the ressource expected. The former realizes the connections between the *Elab* blocks, while the latter implement basic computer vision algorithms that can be part of a specific elaboration pipeline tunable at run-time. This architecture can support multi-camera video inputs that can be parallel processed as a continuous pixel flow. In this respect, the captured flow has not an associated semantic, so that an user interacting with a configuration manager can select and compose the appropriate modules suited to the desired application.

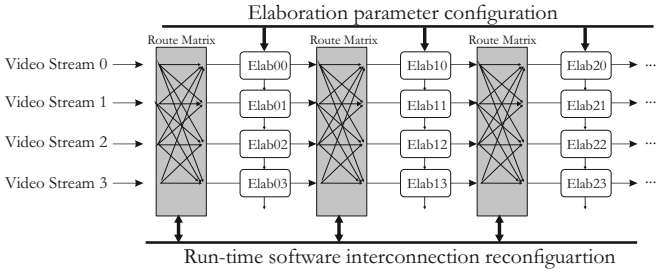

Fig. 3: Configurable processing IP

III. Application

Targeted application is a tracking system in distributed network of smart cameras, presented in Fig 4. Our system will be based on particle filter which is very common for tracking objects [7]. Moreover, Cho et al have demonstrated in [8] that particle filters can be implemented in FPGA device, making us confident about the feasibility of this hardware implementation. A first application (HOG) using this modular architecture has been implemented and the smart camera is currently able to exchange information via Giga-Ethernet communication with low resources FPGA (around 5%). Future development will focus on a wireless transceiver integration and particle filter implementation.

IV. Conclusion

In this paper, we presented a FPGA architecture offering high processing capacity with configurable processing. At this point of the project, we know that out smart camera can autonomously communicate each other on an ethernet network. This first architecture does not take care on low-consumption communication in smart camera network which need to be investigated. A new physical medium is under development and will integrate an IEEE 802.15.4 transceiver supporting wireless communication.

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References

[1] P. Pagano, C. Salvadori, S. Madeo, M. Petracca, S. Bocchino, D. Alessandrelli, A. Azzar, M. Ghibaudi, G. Pellerano, and R. Pelliccia, "A middleware of things for supporting distributed vision applications," in *Proceedings of the 1st Workshop on Smart Cameras for Robotic Applications, SCaBot Workshop*, 2012.

[2] W. W. B. Rinner, *Towards Pervasive Smart Camera Networks*. Academic press, 2009.

[3] P. Chen, P. Ahammad, C. Boyer, S.-I. Huang, L. Lin, E. Lobaton, M. Meingast, S. Oh, S. Wang, P. Yan, A. Yang, C. Yeo, L.-C. Chang, J. D. Tygar, and S. Sastry, "Citric: A low-bandwidth wireless camera network platform," in *Distributed Smart Cameras, 2008. Second ACM/IEEE International Conference on*, 2008.

[4] E. Norouznezhad, A. Bigdeli, A. Postula, and B. Lovell, "A high resolution smart camera with gige vision extension for surveillance applications," in *Distributed Smart Cameras, 2008. ICES 2008. Second ACM/IEEE International Conference on*, 2008, pp. 1–8.

[5] Z. Shelby, K. Hartke, C. Bormann, and B. Frank, "Constrained Application Protocol (CoAP)," CoRE Working Group, Internet Engineering Task Force, October 2012.

[6] M. Birem and F. Berry, "Dreamcam : A modular fpga-based smart camera architecture," in *Journal of System Architecture - Elsevier - To appear - 2013*, 2013.

[7] S. Haykin and N. deFreitas, "Special issue on sequential state estimation," *Proceedings of the IEEE*, vol. 92, no. 3, pp. 399–400, 2004.

[8] J. U. Cho, S.-H. Jin, X. D. Pham, J. W. Jeon, J.-E. Byun, and H. Kang, "A real-time object tracking system using a particle filter," in *Intelligent Robots and Systems, 2006 IEEE/RSJ International Conference on*, 2006, pp. 2822–2827.